et al. in view of Iijima et al. (U.S. Patent No. 5,729,439); rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. in view of Komiyama (U.S. Patent No. 6,424,050); and rejected claims 20 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. and Iijima et al. further in view of Hsuan et al. (U.S. Patent No. 6,236,109).

Applicant respectfully traverses the rejections of claims 3, 12, 13, and 19-25, as detailed above, for the following reasons.

Rejection under 35 U.S.C. § 102(e)

Applicant respectfully traverses the rejection of claims 21-24 under 35 U.S.C. § 102(e) as being anticipated by Sakui et al. for the following reasons.

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102(e), the Examiner must show that each and every element of each of the claims in issue is found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See M.P.E.P. §2131, page 2100-69, 8th Ed., August 2001, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Further, "the elements must be arranged as required by the claim." M.P.E.P. §2131, p. 2100-69.

Independent claim 21 recites a semiconductor device comprising, among other things, "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and a portion of either the first connecting terminals or the second connecting terminals is distributed and arranged on the central area of the

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semiconductor chip, and power source supply potential or ground potential is to be applied thereto."

In the Office Action, the Examiner alleges that Sakui et al. shows "a portion of either the first connecting terminals of *(sic)* the second connecting terminals is distributed and arranged in the central area of the semiconductor chip (a bump 8-4 of the first chip 12-1 in Fig. 3), and power supply (V_{ss}) is to be applied." Office Action at page 8.

Applicant respectfully disagrees with the Examiner's allegations and conclusions because, Applicant submits that the Examiner has mischaracterized the present claimed invention. Specifically, contrary to the Examiner's allegations the bump 8-4 in Sakui et al. does not correspond to the "a portion of either the first connecting terminals or the second connecting terminals is distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential is to be applied thereto," as recited in claim 21.

More specifically, claim 21 recites, among other things, "power source supply potential or ground potential are to be applied **thereto**." (emphasis added). In other words, a power source supply potential or ground potential are to be applied to a portion distributed and arranged on the central area of the semiconductor chip. In contrast, the bump 8-4, as shown in Fig. 3 of Sakui et al. is not connected to either a power source supply potential or a ground potential, as recited in claim 21. Instead, Sakui et al. discloses that chip enable bar signals (CE), i.e., chip selection signals is provided through the bump 8-4. See id. at col. 6, lines 10-14 and Fig. 3.

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Therefore, contrary to the Examiner's allegations, Sakui et al. does not disclose at least a portion of either the first connecting terminals or the second connecting terminals are distributed and arranged on the central area of the semiconductor chip, and power supply potential or ground potential are to be applied thereto, as claimed. Thus, the rejection of claim 21 under 35 U.S.C. § 102(e) is improper, and Applicant respectfully requests the Examiner to withdraw the rejection and the claim be allowed. Applicant submits that claims 22-24 are also allowable at least in view of their dependency from allowable claim 21.

Rejection under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claims 3, 12, 13, 19, 20, and 25 under 35 U.S.C. § 103(a) because a *prima facie* case of obviousness has not been established by the Examiner.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143.

I. Claims 3, 12, 13, and 19 (Sakui et al. and Iijima et al.)

On pages 2-4 of the Office Action, the Examiner rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over over Sakui et al. in view of Iijima et al.

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Claim 3 recites a semiconductor device comprising, among other things, "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be facing to [an] assembly board and the average density of arrangement of **the** one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals." (emphasis added).

The Examiner states that "Fig. 3 [of Sakui et al] shows that the number of the second connecting terminals (7 metal bumps; 8-1 through 8-7) is more than that of the first connecting terminals (five metal bumps) which are formed on the first surface of the chip 12-1." Office Action at page 2. That is, the Examiner alleges that the five bumps in the layer above the bumps 8-1 through 8-7, as shown in Fig 3 of Sakui et al., correspond to claimed "the one of ... terminals," which have an average lower density of arrangement, and bumps 8-1 through 8-7 correspond to the claimed "another ... terminal." However, Applicant respectfully point out that the Examiner has mischaracterized the teachings of Sakui et al. For argument's sake, if one were to accept that the five bumps (as shown in Fig. 3 of Sakui et al.) correspond to "the one of ... terminals," it would be inconsistent to have that set of terminals be "facing to [an] assembly board," as recited in claim 3.

To be more specific, the claimed recitation "**the** one of ... terminal" (which have a lower density of arrangement) (emphasis added) has as its antecedent "one of ... terminals are arranged to be facing [an] assembly board." However, it is impossible to have the connecting terminal layers with the five bumps (as shown in Sakui et al.)

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connected to an assembly board. That is, if one were to accept that the five bumps correspond to the claimed "the one" of the two terminals that has a lower density of arrangement, then those five bumps must also correspond to the connecting terminals that face an assembly board (which is impossible in this case).

In the alternative, if the Examiner is alleging that the bumps 8-1 through 8-7 correspond to the claimed "one of the ... terminals [that are] arranged to be facing to [an] assembly board," then those bumps must also have a lower density of arrangement (which is not true).

Therefore, contrary to the Examiner's allegations, Sakui et al. does not teach or suggest at least "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be facing to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals," as recited in claim 3.

Iijima et al., cited merely to show a flip-chip arrangement, fails to cure the deficiencies of Sakui et al., noted above. Therefore, Sakui et al. and Iijima et al., either taken alone or in combination, fail to teach or suggest at least "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be facing to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another

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of the first connecting terminals and the second connecting terminals," as recited in claim 3.

Further, the Examiner alleges that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Iijima et al. to the device of Sakui et al to have a flip chip arrangement since a flip chip configuration provides a higher density and better performance for a device circuit." Applicant disagrees with the Examiner's allegations and conclusions as an unsubstantiated statement of questionable relevance to Applicant's claimed invention. Applicant further refers the Examiner to the February 21, 2002 Memorandum from USPTO Deputy Commissioner for Patent Examination Policy, Stephen G. Kunin, regarding "Procedures for Relying on Facts Which are Not of Record as Common Knowledge or for Taking Official Notice." In relevant part, the Memorandum states, "If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding" (Memorandum, p. 3). Further, the Memorandum indicates that the Federal Circuit has "criticized the USPTO's reliance on 'basic knowledge' or 'common sense' to support an obviousness rejection, where there was no evidentiary support in the record for such a finding." Id. at 1.

Applicant submits that "[d]eficiencies of the cited references cannot be remedied by the Board's general conclusions about what is "basic knowledge" or "common sense."" In re Lee, 61 USPQ2d 1430, 1432-1433 (Fed. Cir. 2002), quoting In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Should the Examiner maintain the rejection after considering the arguments presented herein, Applicants submit that the Examiner

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must provide "the explicit basis on which the examiner regards the matter as subject to official notice and [allow Applicants] to challenge the assertion in the next reply after the Office action in which the common knowledge statement was made" (Id. at 3, emphasis in original), or else withdraw the rejection.

Therefore, at least because Sakui et al. and Iijima et al., either taken alone or in combination, fail to teach or suggest each and every element of claim 3, the Examiner has failed to establish a *prima facie* case of obviousness for claim 3. Accordingly, the rejection of claim 3 is improper under 35 U.S.C. § 103(a), and Applicant respectfully requests the Examiner to withdraw the rejection of claim 3 and the claim allowed. Applicant submits that claims 12, 13, and 19 are also allowable at least in view of their dependency from allowable claim 3.

II. Claims 3, 12, 13, and 19 (Sakui et al. and Komiyama)

On pages 4-5 of the Office Action, the Examiner rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. in view of Komiyama.

As discussed above regarding the rejection of claim 3, Sakui et al. does not teach or suggest at least "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be facing to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals," as recited in claim 3.

Komiyama fail to cure these deficiencies of Sakui et al. Komiyama discloses a flip chip IC chip with a mounting surface that is externally exposed and is provided with

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external terminals 15. See id. at Fig. 4. The Examiner alleges that Komiyama "clearly show[s] that the density of the conductive bumps arrangement is different between the first connecting terminals 15 and the second connecting terminals 24, 49 of the first chip 1 in Fig. 4." Office Action at page 5. Applicant respectfully disagrees. Without acceding to the Examiner's characterization of Komiyama, if one were to accept, for argument's sake, that terminals 15 correspond to the claimed "the one of ... terminals" that face an assembly board, then still, it is not true that they have an average density of arrangement that is lower than the terminals 24 and 49 (as shown in Komiyama). As can be clearly seen from Fig. 4, terminals 15 are spaced closer than the terminals 24 and 29, and, therefore, are not of a lower average density of arrangement.

Therefore, Sakui et al. and Komiyama, either taken alone or in combination, do not teach or suggest at least "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be facing to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals," as recited in claim 3.

Further, the Examiner alleges that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Komiyama to have a different number of conductive bumps for two connecting terminals in a flip chip configuration in order to have more compact arrangement to reduce a device size." Applicant disagrees with the Examiner's allegations and conclusions as an unsubstantiated statement of questionable relevance to Applicant's claimed invention.

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Applicant submits that "[d]eficiencies of the cited references cannot be remedied by the Board's general conclusions about what is "basic knowledge" or "common sense."" In re Lee, 61 USPQ2d 1430, 1432-1433 (Fed. Cir. 2002), quoting In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Should the Examiner maintain the rejection after considering the arguments presented herein, Applicant submit that the Examiner must provide "the explicit basis on which the examiner regards the matter as subject to official notice and [allow Applicant] to challenge the assertion in the next reply after the Office action in which the common knowledge statement was made" (Id. at 3, emphasis in original), or else withdraw the rejection.

Further to demonstrating that combining the teachings of Sakui et al. with those of Komiyama would not have resulted in Applicant's claimed invention, Applicant respectfully submits that Sakui et al., in fact, teaches away from such a combination. In particular, Sakui et al. discloses a plurality of semiconductor chips of the *same structure* stacked one on another, and option circuits of each semiconductor chip are selected in accordance with the connecting pattern of the metal bumps provided between semiconductor chips. Id. at col. 5, lines 14-19 (emphasis added). Therefore, it would be inconsistent with the teachings of Sakui et al. to incorporate the teachings of Komiyama, which discloses an IC chip 2 mounted in flip-chip configuration and protruded electrodes 49 provided at specified portions of the conductive pattern 47, and are respectively connected to the protruded electrodes 24 formed on a main surface of the IC chip 2. Id. at col. 5, lines 1-11 and Fig. 4.

In summary, the Examiner has failed to establish a *prima facie* case of obviousness for claim 3. Accordingly, Applicant requests the Examiner to withdraw the

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rejection of claim 3 under 35 U.S.C. § 103(a) and the claim be allowed. Applicant submits that claims 12, 13, and 19 are also allowable at least in view of their dependency from allowable claim 3.

III. Claims 20 and 25 (Sakui et al., Iijima et al., and Hsuan et al.)

Claims 20 and 25 contain recitations similar to claims 3 and 21.

Specifically, claim 20 recites, *inter alia*, "one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals." As discussed above regarding the rejection of claim 3, Sakui et al. and Iijima et al. either taken alone or in combination, do not teach or suggest at least the quoted element.

Hsuan et al., cited merely in an attempt to show chips of different sizes, does not cure these deficiencies of Sakui et al. and Iijima et al. Therefore, Sakui et al., Iijima et al., and Hsuan et al., either taken alone or in combination, do not teach or suggest each and every element of claim 20.

Claim 25 recites a semiconductor device comprising, among other things, "a portion of either the first connecting terminals or the second connecting terminals is distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential is to be applied thereto."

As discussed above regarding the rejection of claim 21, Sakui et al. does not teach or suggest at least "a portion of either the first connecting terminals or the second

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connecting terminals is distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential is to be applied thereto," as recited in claim 25.

Iijima et al, cited merely for a flip chip device, and Hsuan et al., cited merely for chips of different sizes, do not cure these deficiencies of Sakui et al. Therefore, Sakui et al., Iijima et al., and Hsuan et al., either taken alone or in combination, do not teach or suggest each and every element of claim 25.

Further, there is no motivation to combine the teachings of the cited references. As discussed above, there is no motivation to combine the teachings of Sakui et al. with those of Iijima et al. In addition, contrary to the Examiner's allegations and conclusions, there is no motivation to combine the teachings of Hsuan et al. with those of Sakui et al. Further to demonstrating that combining the teachings of Sakui et al. with those of Iijima et al. and Hsuan et al. would not result in Applicant's claimed invention, Applicants respectfully submit that Sakui et al., in fact, teaches away from such a combination. In particular, Sakui et al. discloses a plurality of semiconductor chips of the *same structure* stacked one on another, and option circuits of each semiconductor chip are selected in accordance with the connecting pattern of the metal bumps provided between semiconductor chips. Id. at col. 5, lines 14-19 (emphasis added). Therefore, it would be inconsistent with the teachings of Sakui et al. to incorporate chips of different sizes, as taught by Hsuan et al. into the device of Sakui et al. Absent such motivation, clearly there would be no reasonably expectation of success.

Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 20 and 25. Accordingly, Applicant requests the Examiner to

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withdraw the rejection of claims 20 and 25 under 35 U.S.C. § 103(a) and the claims allowed.

Conclusion

In view of the foregoing, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: August 21, 2003

By: Richard V. Burgujian Reg 24,014
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